Power Management IC Simplifies ACPI Implementation (HIP6501AEVAL1)

Application Note | August 1999 | AN9846.2

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Introduction

The Advanced Configuration and Power Interface specification (ACPI; [1]), written by a consortium representing Intel, Microsoft and Toshiba, attempts to evolve the current collection of power management methods and configuration interfaces into a well-specified and unified power management and configuration mechanism. The key objective in the ACPI specification is to transfer all control of power management and configuration functions to the operating system, thus enabling Operating System Directed Power Management (OSPM). ACPI-compliant systems will benefit from a robust interface for configuring motherboard devices, a versatile power management interface enabling a wide variety of solutions with full operating-system support, and not lastly, a realm of new, intelligent possibilities added to the already broad span of PC uses.

The HIP6501A is the first Intersil IC to be used in conjunction with a second chip to provide a complete ACPI-sanctioned motherboard power regulation solution. The HIP6501A/HIP6021 chip sets produce the processor core, GTL bus, memory controller hub, and clock chip voltages, as well as the SDRAM memory, 3.3V and 5V dual voltage planes [2, 3] necessary for a complete PIII-Whitney system implementation.

Quick Start Evaluation

IMPORTANT!

Given the specialized nature of the HIP6501A, the HIP6501AEVAL1 board is meant to be evaluated only with an ATX power supply. Furthermore, only an ACPI-ready ATX supply can be used to power-up the evaluation board (720mA capability on 5VSB output; ATX Specification v2.02, [4]). Standard laboratory power supplies are not suitable for powering up this evaluation board.

Circuit Setup

➤ **Set up JP1 and JP2**

Before connecting the input ATX supply to the HIP6501AEVAL1 board, consult the data sheet and set the JP1 and JP2 configuration jumpers according to the configuration you wish to emulate. This configuration is latched in at power-up, but can be subsequently changed during active state operation (S0, S1) or during a chip shutdown (while PB1 is being pressed). See HIP6501A data sheet for information on all the available configurations and how to set them [5].

➤ **Connect the Input Power Supply**

Ensuring that the supply is not plugged into the mains, or that the AC switch is off (if provided), connect the main ATX output connector to J1.

➤ **Connect the Output Loads**

Connect typical standby loads to all the evaluation board's outputs. Consult Table 1 for maximum loads supported by the design of the HIP6501AEVAL1 in the configuration received; consult the 'HIP6501AEVAL1 Modifications' chapter for information on modifying the evaluation board to meet your special needs.

➤ **Set Start-Up State (Active Is Recommended)**

If start-up in active state is desired, ensure both 'S3' and 'S5' switches are in the off position (away from 'S3' or 'S5' marking). Ensure the 'ATX ON' switch is also in the off position.

Set either the 'S3' or the 'S5' switch for start-up in either of the standby states. IMPORTANT: only one switch needs to be actuated, so select the standby state by turning on the switch with that name - the signal conditioning circuitry ensures correct $\overline{S3}$ and $\overline{S5}$ pin stimulation.

Operation

➤ **Provide Bias Voltage to the Board**

Plug the ATX supply into the mains. If the supply has an AC switch, turn it on. The '5VSB' (LP4) LED should light up, indicating the presence of 5V standby voltage on board.

➤ **Examine Start-Up Waveforms**

Sleep state start-up is immediate following application of bias voltage. Using an oscilloscope or other laboratory equipment, you may study the ramp-up and/or regulation of the controlled voltages, according to the specific JP1, 2 configuration previously set and the specific standby state selected.

For start-up into an active state (standby switches set off prior to application of bias voltage), flip on the 'ATX ON' switch. This will turn on the main ATX outputs and the HIP6501A will start up into active state. Once turned on, SW1 needs not be turned off until bias is removed from the board.

➤ **Examine Output Quality Under Varying Loads**

In either state (sleep or active) vary the output loads to simulate computer loads typical of the specific operating state the circuit is in.

➤ **Examine state transitions**

For subsequent transitions into standby states, leave the main ATX outputs enabled (SW1 on); the circuit will automatically turn them off when entering a standby state. To enter a standby state, turn on the respective switch. The ‘S3’ LED will light up to indicate S3 standby state, while S5 state will illuminate both ‘S3’ and ‘S5’ LEDs. However, the HIP6501A will ignore any illegal transition requests, such as from S3 state to S5 state or vice versa, as shown in Figure 1.

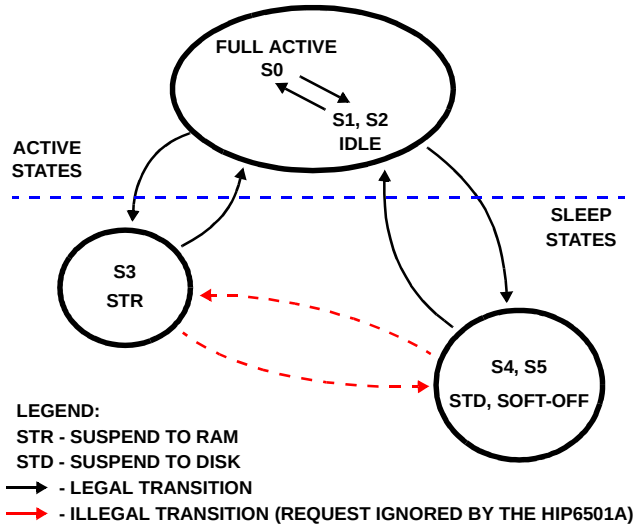


FIGURE 1. HIP6501A LEGAL/ILLEGAL STATE TRANSITIONS

Fault Handling

In case of a FAULT condition (output under-voltage) occurring while in active state (such as a suddenly shorted output), the FAULT/SEL pin assesses a logic ‘high’, shutting down the ATX supply’s main outputs. To recover from such a shutdown, press the ‘SHUTDOWN/CLEAR FAULT’ button (PB1). Depressing PB1 will initiate a soft-start sequence, thus clearing the FAULT, and enabling the main ATX outputs.

If jumper JP3 (FAULT LATCH) is removed, the FAULT output will not latch the circuit. The circuit appears to latch off because the FAULT signal shuts down the ATX supply, cutting off the input supply to the faulting output, and thus keeping it from ever recovering from the fault condition. *However, it is not recommended to test the circuit against output under-voltages (output short-circuits) with JP3 removed*. Due to the very slow response of the ATX supply in response to a shutdown request, the external N/P-MOS switches (Q3A, Q3B, and Q4) in use at the time of testing will usually fail as a result of sustained over-current through the drain-source junction and bond wires. The FAULT latch circuit acts on the SS pin directly, shutting down the IC quickly. To protect the external switches it is recommended that JP3 is shunted throughout the operation of the board.

Configuring Sleep State Support

Sleep state support on the $3.3V_{DUAL}$ and $5V_{DUAL}$ outputs is user-configurable through jumpers JP1 and JP2 (consult data sheet for sleep support details, [5]). The configuration can be changed prior to 5VSB application, during active state operation, as well as during chip shutdown (PB1 pressed). During sleep states, the configuration is latched in and any changes in the $\overline{\text{EN3VDL}}$ and EN5VDL pins’ logic status are ignored.

HIP6501AEVAL1 Reference Design

General

The HIP6501AEVAL1 is built on 2-ounce, 4-layer, printed circuit board (see last three pages of this application note for layout plots). Most of the components specific to the evaluation board alone, which are not needed in a real computer application, are placed on the bottom side of the board. *Assuming the input supplies and the controlled output planes have their own on-board filtering (capacitors), the only components required to implement this ACPI 3-voltage controller/regulator solution are contained within the white rectangle surrounding the HIP6501A on the top side of the board.* All the additional circuitry contained on board has the role of duplicating the computer environment the chip would operate in. Since this additional circuitry would clutter and detract from the readability of the schematic, most of it was grouped in two blocks, named “SIGNAL CONDITIONING” and “FAULT LATCH”.

The board also contains a serpentine resistor which occupies about 1/3 of both top and bottom sides of the board. The ATX supply requires some minimum loading on the +5V output in order to stay active; lack of this minimum loading causes the ATX to shut down all its outputs, except +5VSB. This minimum load is specified as 1A, but most supplies will stay active with as little as 400-500mA. The embedded resistor should draw a current of about 1A (typical). If the current draw is insufficient to keep the power supply active, try reducing the value of the embedded resistor. Shorting out the W1 footprint, on the back side of the board, effectively shorts out 1/4 of the resistive trace, increasing the current draw by 30%. Similarly, shorting out W2 reduces the trace by 50%, thus doubling the current draw from the +5V output. If either W1 or W2 are shorted, it is advised that active state operation be reduced as to avoid severe overheating of the board (in case the 5V current draw exceeds 1A). For most, if not all cases, neither W1 nor W2 need be shorted.

Design Envelope

Although different computer systems might have different requirements, the HIP6501AEVAL1 was designed to meet the maximum output loading described in Table 1. Note the fact that the addition of all the sleep state output currents exceeds the ATX 5VSB output capability (725mA). Real-life sleep state current requirement on each of the outputs could

be lower, and their maximums should rarely all occur simultaneously. Output tolerances and current ratings (with the exception of the 2.5/3.3V_{MEM} output current rating in sleep state) can be adjusted by properly selecting the components external to the HIP6501A.

TABLE 1. HIP6501AEVAL1 MAXIMUM OUTPUT LOADING

OUTPUT VOLTAGE	ACTIVE STATES		SLEEP STATES		TOL. (static/ dynamic)
	I_{OUT}	dI_{OUT}/dt	I_{OUT}	dI_{OUT}/dt	
2.5/3.3V_{MEM}	4A	1A/µs	250mA	1A/µs	5% / 9%
3.3V_{DUAL}	3A	0.2A/µs	600mA	0.2A/µs	9% / 9%
5V_{DUAL}	2.5A	0.1A/µs	200mA	0.1A/µs	9% / 9%

The maximum current draw on the 2.5V_{MEM} output systems employing RDRAM memory) can be as high as 7-8A for short periods of time during memory initialization. To avoid having to design a high-current output which would be used at its fullest potential only during a very short period of time, we recommend reducing the memory clock speed during initialization. This method should result in a significant reduction in the current needed during initialization. This current can then be delivered through a single external pass transistor connected directly to the DRV2 pin.

HIP6501AEVAL1 Performance

Figures 2-6 depict the evaluation board's performance during a few typical operational situations. To simulate minimum loading conditions, unless otherwise specified, the outputs were loaded with 65Ω resistive loads.

Sleep-State Start-Up

Figure 2 shows a typical start-up into S3 sleep state while all outputs are enabled ($\overline{EN3VDL}$ = 0, EN5VDL = 1). As 5VSB is applied to the board, SW1 and SW3 are off, while SW2 is on. At time T0 the input supply exceeds the power-on-reset (POR) threshold. Three milliseconds afterwards, at time T1, the soft-start clamp is removed and the outputs start to ramp up toward their target value, which they reach at time T2. The 5V_{DUAL} output has a slightly different ramp-up due to the fact that it undergoes a different soft-start than the remainder of the output voltages. The 5V_{DUAL} output is not actively regulated, as is the case with the 2.5V_{MEM} and 3.3V_{DUAL} outputs in S3, but rather switched on through a P-MOS or PNP switch. An error amplifier is thus provided for the 5V_{DUAL} output just for the purpose of providing a smooth, controlled output voltage rise. This error amplifier uses a different, soft-start derived, control signal to achieve the controlled ramp-up of the output.

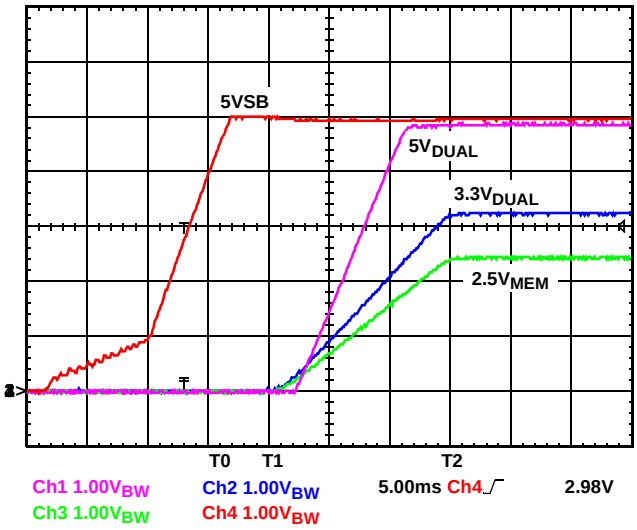


FIGURE 2. HIP6501AEVAL1 START-UP IN SLEEP STATE (S3) WITH ALL OUTPUTS ENABLED

Active-State Start-Up

Figure 3 also shows a start-up sequence, but this time into active state (S0,S1). As the enable pins only configure the sleep state voltage support, this start-up sequence will be the same, regardless of $\overline{EN3VDL}$ and EN5VDL status. In Figure 3, SW1, SW2 and SW3 are all off and 5VSB is applied to the board. Active state operation is enabled by switching on SW1, just 3-4ms before T0. At time T0, the 12V input exceeds the under-voltage threshold and the internal 50ms (typical) timer is initiated. Between T0 and T1, the 3.3V_{DUAL} and 5V_{DUAL} outputs undergo a quasi soft-start, due to conduction through the body diodes of the active N-MOS switches (Q3A and Q3B). At time T1 the timer expires and the two N-MOS transistors are turned on; simultaneously the 2.5V_{MEM} output begins a soft-start cycle, being charged up through the external pass transistor, Q1.1B. The ramp-up of the 2.5V_{MEM} output ends at T2, when it reaches its regulation limit.

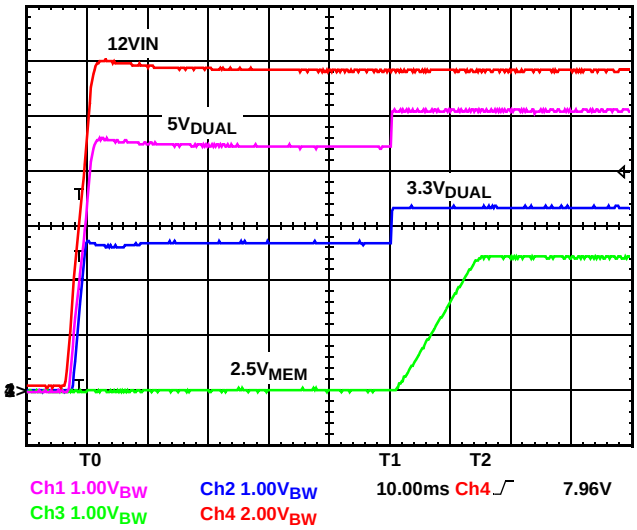


FIGURE 3. HIP6501AEVAL1 START-UP IN ACTIVE STATE (S0,S1) WITH ALL OUTPUTS ENABLED

State Transition

Figure 4 shows the transition from active state (S0,S1) to S3 sleep state. Prior to time T0, the evaluation board was operating in active mode, with SW1 on and SW2 and SW3 off. At time T0, SW2 is switched on, triggering the switch-over of the output regulation from the active ATX output rails to the 5VSB supply, as well as the turn-off of the ATX. At time T1 the ATX responds to the turn-off request, and the 5V output starts to ramp down under the current draw caused by the embedded 5Ω serpentine resistor.

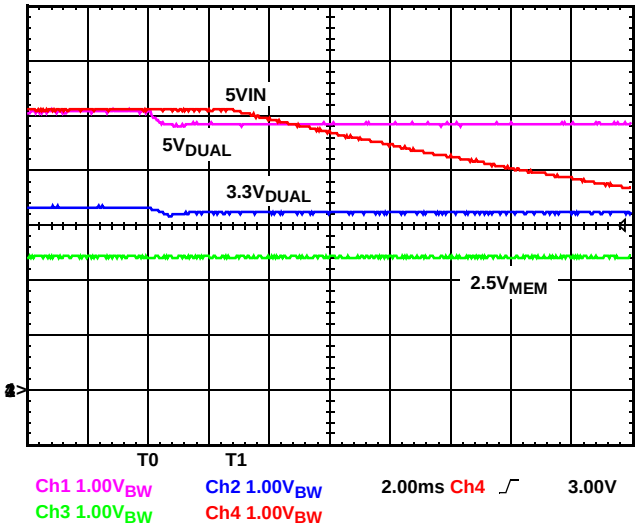


FIGURE 4. HIP6501AEVAL1 ACTIVE STATE (S0,S1) TO STANDBY STATE (S3) TRANSITION WITH ALL OUTPUTS ENABLED

The transition back from S3 sleep state to active state mirrors the active-to-sleep state transition, above.

Transient Response

In Figure 5, all the outputs of the evaluation circuit are subjected to simultaneous load transients while operating in active state (S0, S1). Output loading of each output consists of different frequency transients of amplitude equal to the maximum active state current as defined in Table 1, superimposed on a constant 50mA load. The output transients' rate of change (dI/dt) also match the values described in Table 1. All outputs shown in the oscilloscope capture are DC offset by their nominal value, and all are DC coupled. The rectangles underneath each of the output waveforms indicate the duration of each transient occurring on the respective output.

As it can be seen in Figure 5, the $3.3V_{DUAL}$ output follows the AC meandering of the ATX 3.3V output very accurately, being separated only by the $r_{DS(ON)}$ of the N-MOS switch (Q3A). During the transient loading, the 3.3VDUAL output develops a DC offset, due to the voltage droop across Q3A. Specific to this circuit and the particular circuit loading, the offset can easily be identified as the product of 50mΩ and 3A, resulting in 150mV of voltage drop.

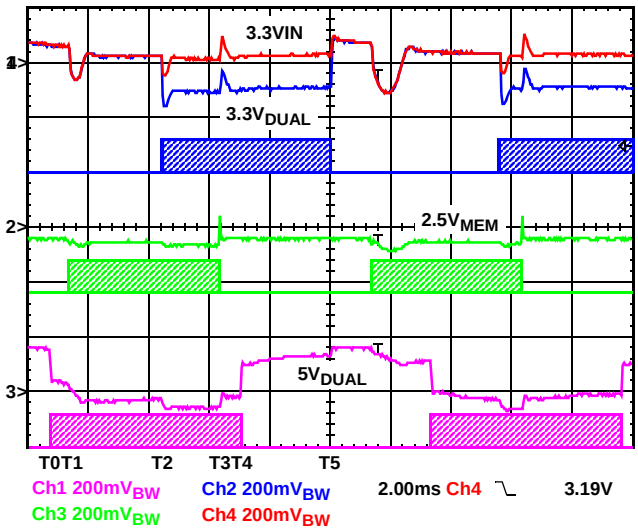


FIGURE 5. HIP6501AEVAL1 ACTIVE STATE (S0,S1) OUTPUT TRANSIENT RESPONSE (ALL OUTPUTS ENABLED)

Similar explanation accompanies the 5VDUAL output waveform, except that the ATX 5V output could not be shown due to measurement equipment limitations. However, the voltage offset caused by the transient load application can be identified as the product of 50mΩ and 2.5A, resulting in 125mV of voltage droop.

The situation is different with the 2.5VMEM output.

This output is actively regulated by the IC, and the resulting output regulation is a combined effect of high dV/dt ripple caused by the transient edges, decreased voltage overhead for the pass NPN transistor due to ATX 3.3V ripple, as well as DC accuracy of the internal circuitry. Under the combined effects of all parameters listed above and with fairly scarce amounts of capacitance present on board, the memory output is still maintained within a 4% tolerance.

Output Short-Circuit Protection

Figure 6 depicts the circuit's behavior in response to a sudden output short-circuit (output under-voltage), applied in this scope capture on the $2.5V_{MEM}$ output, while operating in active state. At time T0 a short-circuit is applied using an electronic load - as a result, the 2.5V output starts to rapidly discharge, crossing the falling under-voltage threshold (68% of 2.5 = 1.7V) at time T1. To avoid false triggers, the UV detector is equipped with a 10µs filter. As the UV event exceeds the 10µs window, it triggers a fault response at time T2. The logic high output on the FAULT/MSEL pin sets the external fault latch circuitry which quickly discharges the SS capacitor just below the chip shutdown level, reached at time T3. The chip reset disables the fault reporting and the latch maintains the circuit in a reset state. Depressing the CLEAR FAULT button resets the latch and releases the circuit for operation.

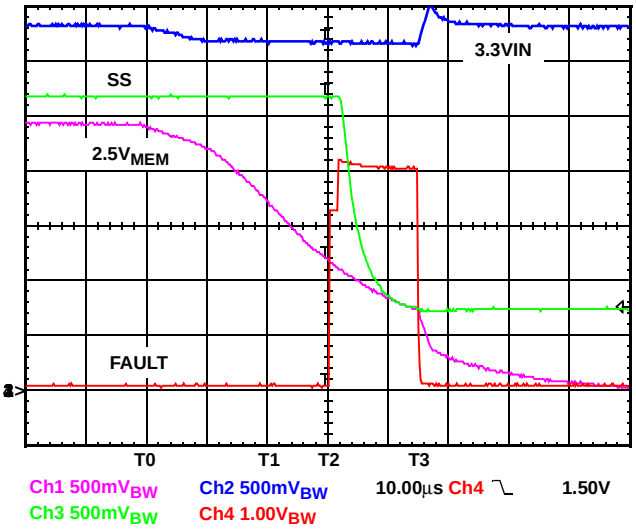


FIGURE 6. HIP6501AEVAL1 2.5V_{MEM} OUTPUT UNDERVOLTAGE RESPONSE WHILE IN ACTIVE STATE (S0, S1))

HIP6501AEVAL1 Modifications

Setting the 2.5/3.3V_{MEM} Output to 3.3V

The HIP6501AEVAL1 evaluation board ships populated for RDRAM memory support, with the memory output set for 2.5V. The HIP6501A, however, is designed for either 2.5V or 3.3V memory output voltage. To change the memory output voltage on the evaluation board perform the following steps:

- Remove Q1.1B, or lift both base and emitter pins off the solder pads on the board
- Replace R3 with a 15kΩ resistor
- Install an N-MOS, SO-8 transistor, HUF76113SK8 or equivalent, in the provided Q1.2 footprint

With the above modifications, the memory output will be set to 3.3V. In this configuration, the output voltage obtainable in active state is directly related to the ATX 3.3V output, the memory output current, and the $r_{(DS)ON}$ of Q1.2, according to the following equation:

$$V_{MEM} = V_{IN} - I_{MEM} \times r_{(DS)ON}$$

Improving Output Voltage Tolerance

The key to improving the output voltage tolerance is identifying the parameters which affect it, and then taking steps toward improving them.

As explained in the text accompanying Figure 5, the output DC voltage droop on the 3.3V_{DUAL} and 5V_{DUAL} outputs under applied load is due to the resistive losses across the N-MOS switch's own $r_{DS(ON)}$ - decreasing the $r_{DS(ON)}$ results in reduced load-dependent voltage droop.

High dV/dt spikes present in the output voltage waveform under highly dynamic load application (high dI/dt) are due to the ESR and the ESL of the output capacitance. These spikes coincide with the transient load's rising and falling edges, and decreasing their amplitude can be achieved by using lower ESR/ESL output capacitors (such as surface-mount tantalum capacitors), and/or the addition of more ceramic capacitors, which have inherently low ESR/ESL.

The addition of more input-side capacitance and decreasing the input-side capacitor banks' ESR can also help in situations where the input-side ripple is affecting the output regulation. Such an example is the 3.3V ripple reducing the overhead voltage available for Q1.1B, and thus inducing an output droop component - in such instance, the addition of input-side capacitance and reduction of the ESR component can reduce the output excursion.

Conclusion

The HIP6501A is a sophisticated integrated circuit that envelops all the required circuitry for ease of ACPI implementation. The circuit employs intelligent switching methods for smooth power plane transitions, noise immunity circuitry for nuisance trip avoidance, and a direct interface to the south bridge and logical circuitry for simplified control and configuration.

References

For Intersil documents available on the internet, see web site http://www.intersil.com/

[1] Advanced Configuration and Power Interface Specification, Revision 1.0, December 1996, Intel/Microsoft/Toshiba. (http://www.teleport.com/~acpi/).

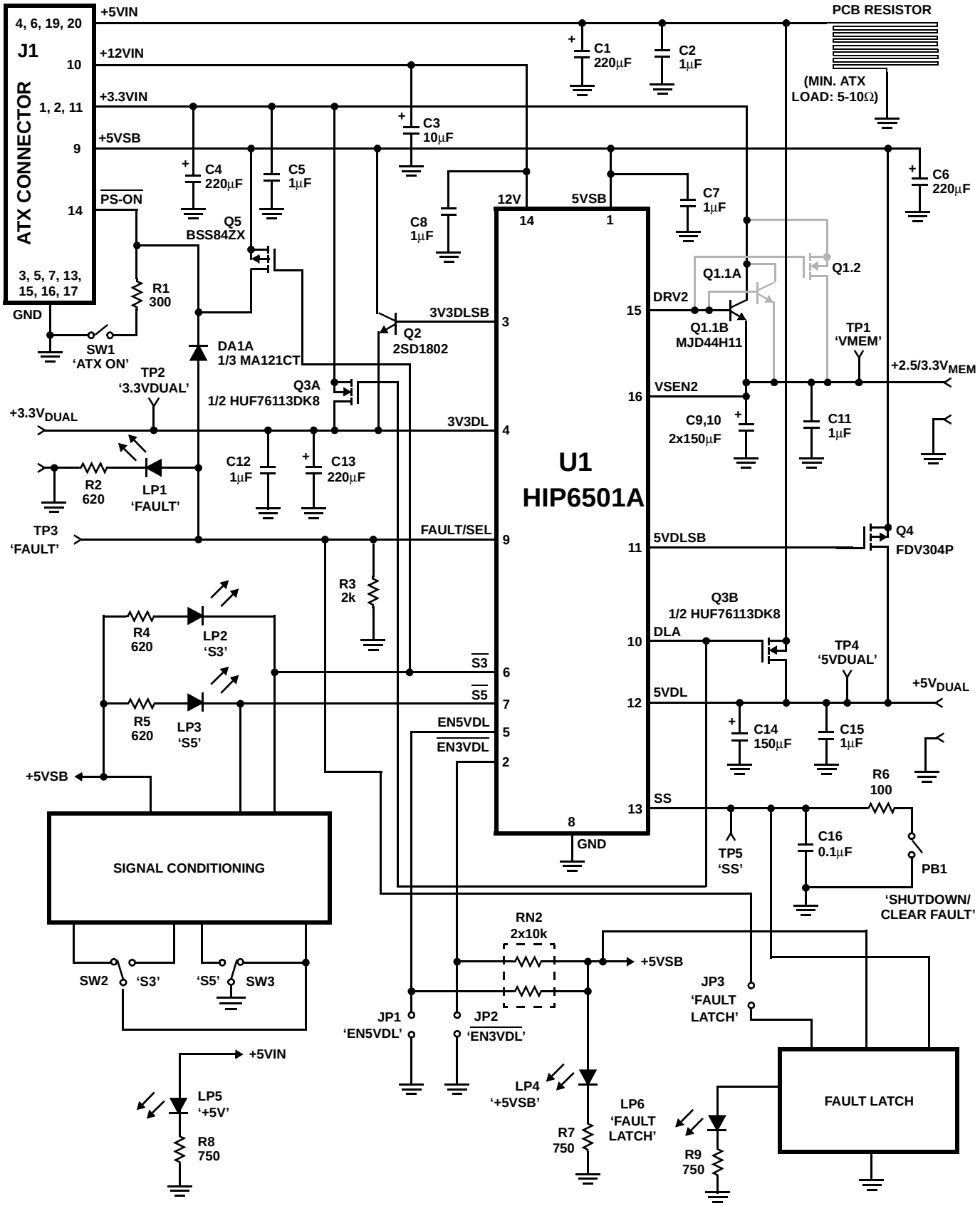
[2] *HIP6020 Data Sheet,* Intersil Corporation, Document No. FN4683, 1999. (http://www.intersil.com/).

[3] *HIP6021 Data Sheet,* Intersil Corporation, Document No., FN4684, 1999.

[4] ATX Specification, Version 2.02, October 1998, Intel Corporation (http://www.teleport.com/~atx/).

[5] *HIP6501A Data Sheet,* 1999, Intersil Corporation, Document No. FN4749.

HIP6501AEVAL1 Schematic



Bill of Materials for HIP6501AEVAL1

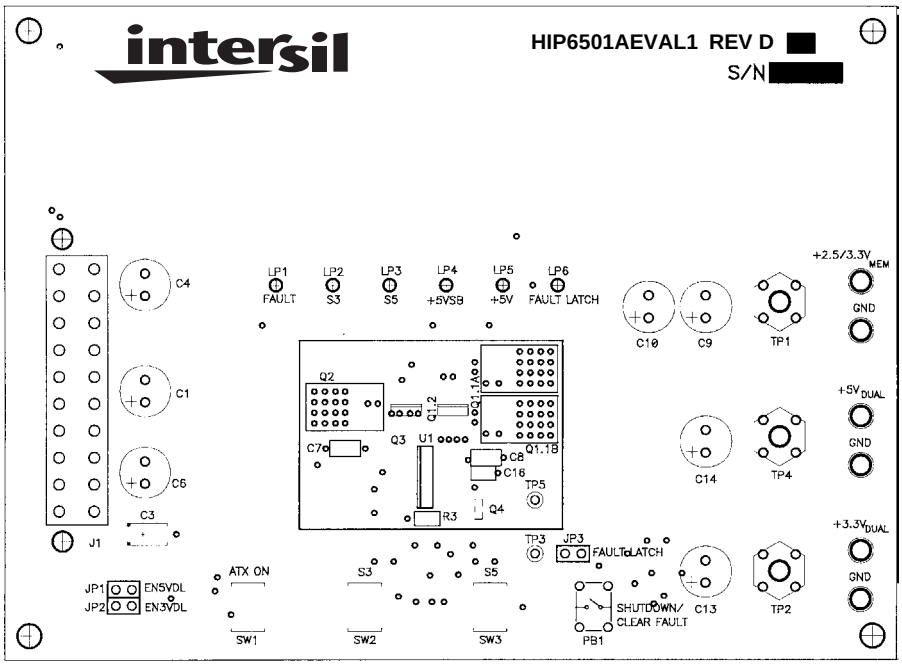
REF	PART #	DESCRIPTION	PACKAGE	QTY	VENDOR
C1, 4,6, 13	EEUFC1E221	Aluminum Electrolytic Capacitor, 25V, 220µF, 117mΩ	8 x 11.5	4	Panasonic
C3	TAJC106M020R	Tantalum Capacitor, 20V, 10µF, 2Ω	3.2 x 6.0	1	AVX
C2, 5, 7, 8, 11, 12, 15	1µF Ceramic	Ceramic Capacitor, Y5V, 16V, 1.0µF	0805	7	Any
C9,10,14	EEUFC1V151	Al. Electrolytic Capacitor, 35V, 150µF, 117mΩ	8 x 11.5	3	Panasonic
C16	0603YC104MAT2A	Ceramic Capacitor, X7R, 16V, 0.1µF	0603	1	AVX
D1	MA732CT-ND	Schottky Diode, 30V, 30mA	Mini 2P	1	Digikey
DA1-3	MA121CT-ND	Diode Array, 80V, 100mA	Mini 6P	3	Digikey
J1	39-29-9203	20-pin Mini-Fit, Jr.™ Header Connector		1	Molex
JP1-3	68000-236	Jumper Header	0.1” spacing	6/36	Berg
	71363-102	Jumper Shunt	0.1” spacing	3	Berg
LP1-6	L63111CT-ND	Miniature LED, Through-Board Indicator		6	Digikey
PB1	P8007S-ND	Push-Button, Miniature		1	Digikey
Q1.1A (Note 2)	Spare		TO-252AA		
Q1.1B (Note 2)	MJD44H11	NPN Bipolar, 80V, 8A	TO-252AA	1	Motorola
Q1.2 (Note 2)	HUF76113SK8	UltraFET™ MOSFET, 30V, 30mΩ	SO-8		Intersil
Q2	2SD1802	NPN Bipolar, 50V, 3A	TO-252AA	1	Sanyo
Q3A, B	HUF76113DK8	Dual UltraFET™ MOSFET, 30V, 32mΩ	SO-8	1	Intersil
Q4	FDV304P	Logic P-MOSFET, 25V, 1.5Ω	SOT-23	1	Fairchild
Q5	BSS84ZXCT-ND	Logic P-MOSFET, 50V, 10Ω	SOT-23	1	Digikey
QA1, 2	ZDM4206NCT-ND	Small-Signal Dual MOSFET, 60V, 1Ω	SM-8	2	Digikey
QA3	ZDT6718CT-ND	Small-Signal Bipolar Pair, 20V, 1.5A	SM-8	1	Digikey
R1	300Ω	Resistor, 5%, 0.1W	0603	1	Any
R2, 4, 5	620Ω	Resistor, 5%, 0.1W	0603	3	Any
R3 (Note 1)	2.0kΩ	Resistor, 5%, 0.1W	0603	1	Any
R6	100Ω	Resistor, 5%, 0.1W	0603	1	Any
R7, 8, 10	750Ω	Resistor, 5%, 0.1W	0603	3	Any
R9, 11	1.0kΩ	Resistor, 5%, 0.1W	0603	2	Any
RN1, 3	Y9103CT-ND	4-Resistor Network, 10kΩ, 5%, 0.1W	3.2 x 1.6	2	Digikey
RN2	Y8103CT-ND	2-Resistor Network, 10kΩ, 5%, 0.1W	1.6 x 1.6	1	Digikey
SW1	GT12MSCKE	Miniature Switch, Single Pole, Single Throw		1	C&K
SW2, 3	GT11MSCKE	Miniature Switch, Single Pole, Double Throw		2	C&K
TP1, 2, 4	1314353-00	Test Point, Scope Probe		3	Tektronics
TP3, 5	SPCJ-123-01	Test Point		2	Jolo
U1	HIP6501ACB	ACPI Triple Linear Controller	SOIC-16	1	Intersil
GND, +3.3V_{DUAL}, +5V_{DUAL}, +2.5/3.3V_{MEM}	1514-2	Terminal Post		6	Keystone

NOTES:

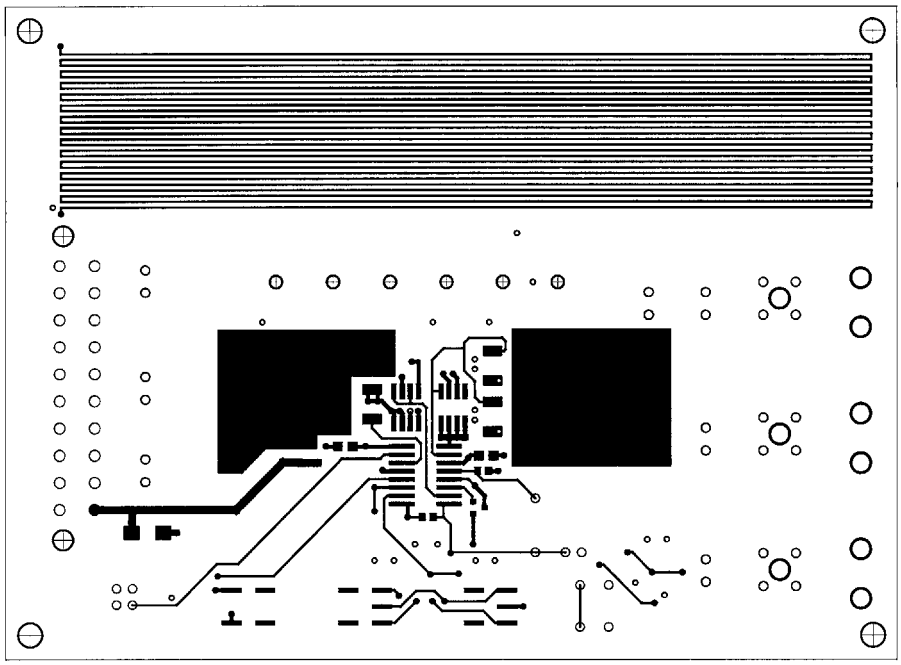
1. R3 has to be 15kΩ when 3.3V V_{MEM} output is desired.
2. Q1.1B and Q1.1A (if present) have to be removed and Q1.2 (or equivalent) has to be populated when R3 = 15kΩ (V_{MEM} set for 3.3V).

HIP6501AEVAL1 Layout (Top Silk Screen and Top Layer)

TOP
SILK SCREEN

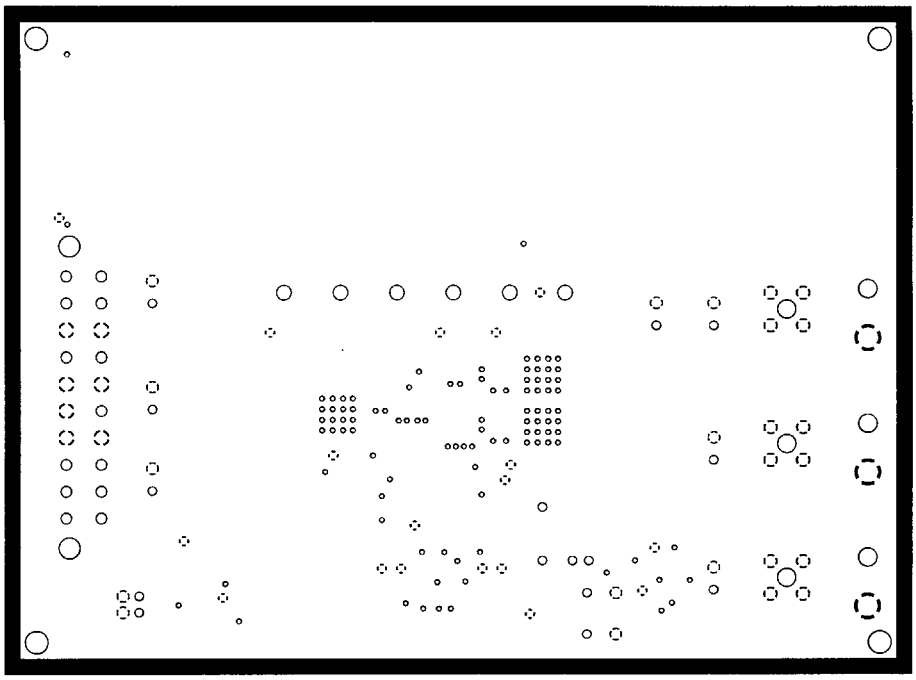


TOP LAYER

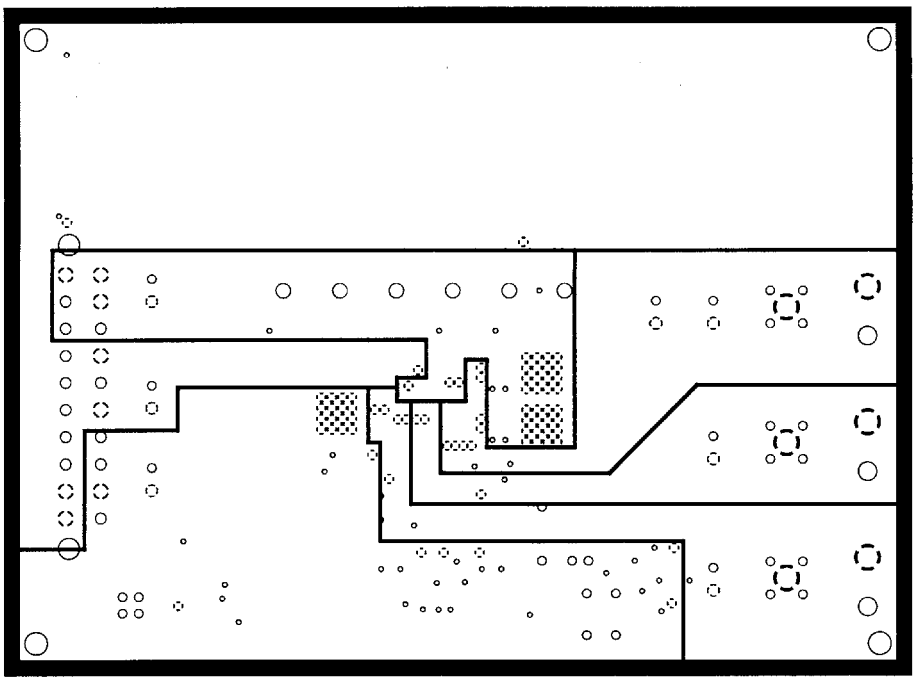


HIP6501AEVAL1 Layout (Ground Layer and Power Planes Layer)

INTERNAL 1
GND

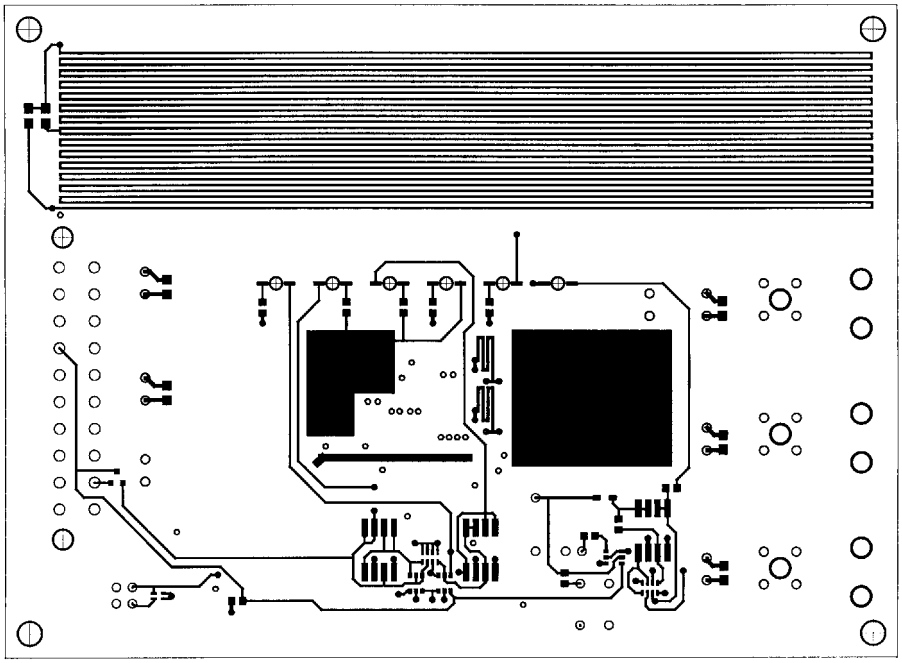


INTERNAL 2
PWR



HIP6501AEVAL1 Layout (Bottom Layer and Bottom Silk Screen)

BOTTOM LAYER



BOTTOM SILK SCREEN